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APPLICATION FOR LETTERS PATENT

for

LOW-POWER, LOW-NOISE CMOS AMPLIFIER

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LOW-POWER, LOW-NOISE CMOS AMPLIFIER

[01] FIELD OF THE INVENTION

[02] The invention generally relates to devices and methods for amplifying electric signals. More specifically, the invention relates to devices and methods for amplifying weak electric signals using a low-power, low-noise amplifier. In particular, the invention relates to a devices and methods for amplifying weak electric signals using an amplifier that is fully integrated in a standard CMOS process and that is capable of rejecting large DC offsets while amplifying signals down to the sub-Hz range.

[03] BACKGROUND OF THE INVENTION

[04] In recent years, there has been an increasing need for technologies that enable neuroscientists and medical personnel to observe the electrical activity in humans and animals, e.g., the neural activity (or activity of neurons) in the brain. Such neural activity is typically observed using recording systems and techniques containing—among other equipment—multi-electrode arrays and amplifying systems. Such recording systems and techniques are becoming standard in basic neuroscience research and the knowledge gained from such systems and techniques are enabling numerous clinical and neuroprosthetic applications.

[05] Recent advances in MEMS technology have produced small (less than 4mm in any dimension) arrays of microelectrodes containing up to 100 neural recording sites.

Future generations of arrays with hundreds and even thousands of electrodes are currently being developed. This desired improvement has increased the need for smaller and more powerful amplifying systems to work in conjunction with the improved microelectrode arrays.

[06] Integrated electronic technologies have been developed for more powerful amplification systems that allow small-scale amplification of weak bioelectrical signals. Such integrated electronic technologies are exemplified in, for example: Degrauwe et al. "A Micropower CMOS-Instrumentation Amplifier" *IEEE J. Solid-State Circuits* 20: 805-807, 1985; Van Peteghem et al. "Micropower High-Performance SC Building Block For Integrated Low-Level Signal Processing" *IEEE J. Solid-State Circuits* 20: 837-844, 1985; Dorman et al. "A Monolithic Signal Processor For a Neurophysiological Telemetry System" *IEEE J. Solid-State Circuits* 20: 1185-1193, 1985; Najafi et al. "An Implantable Multielectrode Array With On-Chip Signal Processing," *IEEE J. Solid-State Circuits* 21: 1035-1044, 1986; Steyaert et al., "A Micropower Low-Noise Monolithic Instrumentation Amplifier For Medical Purposes," *IEEE J. Solid-State Circuits* 22: 1163-1168, 1987; Metting van Rijn et al. "High-Quality Recording of Bioelectric Events," *Med. & Biol. Eng. & Comput.* 29:1035-1044, 1986; Ji et al. "An Implantable CMOS Circuit Interface For Multiplexed Microelectrode Recording Arrays," *IEEE J. Solid-State Circuits* 27: 433-443, 1992; Pancrazio et al. "Description and Demonstration of a CMOS Amplifier-Based-System With Measurement and Stimulation Capability For Bioelectrical Signal Transduction" *Biosensors & Bioelectronics* 13: 971-979, 1998; Martins et al. "A CMOS

IC For Portable EEG Acquisition Systems," *IEEE Trans. Instrument. and Measurement* 47: 1191-1196, 1998; and Steyaert et al. "Low-Noise Monolithic Amplifier Design: Bipolar Versus CMOS" *Analog Integrated Circuits and Signal Processing* 1: 9-19, 1991.

[07] Unfortunately, existing amplification systems based on such integrated electronic technologies typically have either unacceptable noise levels or consume too much power to be fully implantable in large quantities, which will become necessary for the next generation of amplification equipment, especially those used to record neural or other biopotential signals. Extracellular neural signals have amplitudes ranging from 10μV to 10mV and with typical electrode impedances between 100kΩ and 1MΩ at 1kHz. Due to electrochemical effects at the electrode-tissue interface, DC offsets of 1-2V are common between differential recording electrodes. Neural "spikes" often contain energy in the 100Hz – 7kHz band and the energy of local field potentials (LFPs) extends below 1Hz.

[08] To operate under these conditions, some existing VLSI bioamplifier designs use off-chip capacitors—separate form the chip containing the remainder of the amplifier circuit—in the nF range, thereby obtaining a low-frequency cutoff that passes LFP signals while rejecting large dc offsets. This approach, however, is not feasible for large numbers of implanted electrodes that will be necessary for the next generation of recording systems because of size considerations.

[09] SUMMARY OF THE INVENTION

[10] The invention provides devices and methods for amplifying weak electric signals. The device of the invention includes an amplifier that is fully integrated in a standard CMOS process and is capable of rejecting large DC offsets while amplifying signals down to the sub-Hz range. This result is achieved by using single-transistor MOS "pseudo-resistor" elements to achieve a very low cutoff frequency in the mHz range or lower. When combined with an electrode array or sensor array, the fully-integrated amplifier is suitable for recording biological and biopotential signals from the mHz range up to and including about 7kHz. The amplifier also rejects DC offsets at the input and offers a superior power-noise tradeoff than other amplifiers currently available.

[11] BRIEF DESCRIPTION OF THE DRAWINGS

[12] Figures 1-8 are views of devices and methods for amplifying weak electric signals according to the invention, in which:

[13] Figure 1 illustrates one aspect of an amplifier according to the invention;

[14] Figure 2 illustrates the current-voltage relationship of a transistor component in an amplifier of the invention;

[15] Figure 3 depicts another aspect of an amplifier according to the invention;

[16] Figure 4 shows the transfer function of an amplifier according to the invention;

[17] Figure 5 depicts an amplifier's response to a low-frequency square wave in one aspect of the invention;

[18] Figure 6 illustrates an amplifier's noise power spectral density in one aspect of the invention;

[19] Figure 7 depicts an amplifier's input-referred noise as a function of time in one aspect of the invention; and

[20] Figure 8 depicts a comparison of current against noise curves for various known amplifiers and an amplifier according to one aspect of the invention.

[21] Figures 1-8 presented in conjunction with this description are views of only particular—rather than complete—portions of devices and methods for amplifying weak electric signals according to the invention.

[22] DETAILED DESCRIPTION OF THE INVENTION

[23] The following description provides specific details in order to provide a thorough understanding of the invention. The skilled artisan will understand, however, that the invention can be practiced without employing these specific details. Indeed, the invention can be practiced by modifying the illustrated apparatus and method and can be used in conjunction with apparatus and techniques conventionally used in the industry. For example, the invention is described with respect to devices and methods for amplifying weak bioelectric signals. The invention described below, however, could be easily modified for any weak electric signals regardless of the source.

[24] The invention includes a system for recording electrical signals. In one aspect of the intention, the system records bioelectrical signals using a sensor array (including an

electrode array) and an amplifying system. The amplifying system contains an amplifier that is fully-integrated and able block the DC offsets while simultaneously maintaining the low-frequency information often contained in weak bioelectric signals.

[25] Many biological signals (not to mention signals from many types of non-biological signals) are contained in low-frequency ranges (mHz to low Hz range). Many of these signals have important information in this low-frequency range, but are difficult to analyze and use because they also have large DC offsets. Many in the art have found it difficult using fully-integrated circuits to block the DC offsets while simultaneously maintaining the low-frequency information. Instead, they use off-chip capacitors to perform this function. Because the amplifier of the invention does not use off-chip capacitors, the amplifying system of the invention can be much smaller than those currently available.

[26] The invention can be used for many types of electrical signals. In one aspect of the invention, the electrical signals are biological in nature (or bioelectrical signals). Such biological-based signals or bioelectrical signals would include: neural signals: biopotential signals like EMGs, EKGs, and EGGs; or other muscle signals. When used with such signals, the amplifiers are referred to as biosignal amplifiers, or bioamplifiers.

[27] Any fully-integrated amplifying system that blocks DC offsets while simultaneously maintaining the low-frequency information in these low-frequency ranges can be used in the invention. In the invention, a "fully-integrated" amplifier is one in which all of the components of the amplifier—such as capacitors and transistors—are

manufactured on a single chip. In one aspect of the invention, the amplifier depicted in Figure 1 is employed in the invention. Figure 1 is a schematic illustration of the circuit topology of this exemplary amplifier. The midband gain A_M of the amplifier is determined, in part, by the C_1/C_2 ratio. The gain of amplifier can generally range from about 1 to about 1000. Preferably, the gain of the amplifier ranges from about 20 to about 100.

[28] In one aspect of the invention, the bandwidth of the amplifier can be represented by $g_m/(A_M C_L)$, where g_m is the transconductance of the operational transconductance amplifier (OTA). The upper bandwidth limit of the amplifier of the invention can generally range from about 1Hz to about 100kHz. Preferably, the upper bandwidth limit of the amplifier ranges from about 30Hz to about 30kHz.

[29] In the aspect of the invention illustrated in Figure 1, transistors M_a, M_b, M_c, and M_d are MOS-bipolar devices acting as "pseudo-resistors". In other words, with a negative voltage V_{GS}, these transistors function as diode-connected *p*MOS devices. And with a positive voltage V_{GS}, the parasitic source-well-drain *pnp* bipolar transistor is activated, and the device acts as a diode-connected bipolar device as illustrated in Figure 2. Any transistor known in the art functioning in this manner can be employed as the M_a, M_b, M_c, and M_d transistors. In one aspect of the invention, each transistor is any single-transistor MOS "pseudo-resistor" element, such as those described in U.S. Patent No. 5,376,813 as an adaptive element. Unlike that patent, the invention does not use this single-transistor

for nonlinear adaptation. Instead, the transistor acts as a linear pseudo-resistor to achieve a very low cutoff frequency in the mHz range or lower.

[30] The incremental resistance of the amplifier of the invention is relatively high. And for small voltages across the amplifier, the incremental resistance r_{inc} is extremely high. For example, for the amplifier illustrated in Figure 1 and with an absolute voltage differential $|\Delta V|$ less than about 0.2V, the incremental resistance dV/dI is greater than $10^{11}\Omega$. Preferably, the incremental resistance of the amplifier of the invention can be greater than about 10^{11} Ω. For larger voltage differentials, such as 0.4V, the incremental resistance can range from about 10^{9} to about 10^{11} Ω.

[31] The amplifier of the invention can also reduce distortion for large output signals. In the aspect of the invention depicted in Figure 1, two MOS-bipolar devices (M_a and M_b or M_c and M_d) are configured in series to reduce distortion for large output signals, e.g., signals having a voltage amplitude ranging from about 500mV to about 1V. In the aspect of the invention depicted in Figure 1, the low-frequency cutoff ω_L can be represented by $1/(2r_{inc}C_2)$.

[32] The OTA that can be used in the amplifier depicted in Figure 1 can be any known in the art. The OTA uses any configuration of transistors that is suitable for driving capacitive loads, such as that configuration illustrated in Figure 3 with transistors M_1 through M_{10}. The sizing of the transistors (width-to-length ratio, or W/L ratio), however, should be selected to achieve low noise at low current levels. In one aspect of the invention, the transistor sizes are selected to obtain an input-referred noise ranging from

about 2.2 to about 3.6μVrms when the bias current ranges from about 5 to about 20μA. Accordingly, as described in more detail below, the transistor *W/L* ratio can range from about 100 to about 800 for transistors M_1 and M_2, from about 0.13 to about 0.5 for transistors M_3-M_6, and from about 0.13 to about 1 for transistors M_7 and M_8. Preferably, the transistor *W/L* ratio range is from about 150 to about 250 for transistors M_1 and M_2, from about 0.2 to about 0.4 for transistors M_3-M_6, and from about 0.25 to about 0.75 for transistors M_7 and M_8. In one aspect of the invention, the transistors may operate in either weak or strong inversion depending on their *W/L* ratio.

[33] In one aspect of the invention, transistors M_1-M_8 have the same DC drain current. In this aspect of the invention, the transistors M_1 and M_2 (which operate as input devices in the OTA) can be configured with substantially similar sizes with a transconductance of g_{m1} and a width-to-length ratio of $(W/L)_1$. Likewise, transistors M_3-M_6 can be configured with substantially similar sizes $(W/L)_3$ with a transconductance g_{m3}. The transistors M_7 and M_8 can be *p*MOS current mirror transistors and have substantially similar sizes $(W/L)_7$ with a transconductance g_{m7}.

[34] Given these sizes and transconductances, the input-referred thermal noise power of the circuit depicted in Figure 3 can be represented by formula (1):

$$\overline{v_{ni,\text{thermal}}^2} = \frac{8kT\gamma}{g_{m1}}\left[1 + 2\frac{g_{m3}}{g_{m1}} + \frac{g_{m7}}{g_{m1}}\right] \qquad (1).$$

By carefully selecting the *W/L* ratios of the respective transistors so that both g_{m3} and g_{m7} are substantially less than g_{m1} (i.e., by a factor of about 10 to 20), the noise contributions of transistors M_3 through M_8 can be substantially reduced, e.g, by about 4. This "noise

reduction" can be accomplished by making the W/L ratios of transistors M_3-M_6 $[(W/L)_3]$ and the W/L ratios of transistors M_7 and M_8 $[(W/L)_7]$ substantially less than the W/L ratios of transistors M_1 and M_2 $[(W/L)_1]$, thereby pushing transistors M_3-M_8 into strong inversion (because their relative transconductance g_m/I_D in strong inversion decreases as $1/\sqrt{I_D}$).

[35] In certain aspects of the invention, it can be difficult to increase g_{m3} and g_{m7} arbitrarily without risking instability. When the capacitance seen by the gate of transistor M_3 (or M_4) is C_3, then the OTA illustrated in Figure 3 has two poles at g_{m3}/C_3 and at g_{m7}/C_7. To increase stability, these two pole frequencies must be greater—and preferably several times greater—than the dominant pole g_{m1}/C_L. This condition becomes easier to accomplish as the capacitance C_L becomes larger, but this requires consideration of area limitations and bandwidth requirements.

[36] The W/L ratios of the transistors is a tradeoff of several factors. The W/L ratio of the transistors M_3 through M_8 $[(W/L)_3$ and $(W/L)_7]$ should be minimized as much as possible, thereby trading off phase margin for lower input-referred noise. However, the transistor gate area $W \cdot L$ should be as large as possible to minimize $1/f$ noise. But as transistors M_3 through M_8 are made larger, C_3 and C_7 increase, leading to a reduced phase margin. As well, as transistors M_1 and M_2 are made with larger gate areas, the input capacitance C_{in} of the OTA (illustrated in Figure 3) increases, resulting in more OTA noise.

[37] In light of these tradeoffs, an optimum transistor size in the invention was determined in the following manner. To minimize noise within a given power range, the

tradeoff between power and noise was quantified by the noise efficiency factor (NEF) represented by formula (2):

$$\mathrm{NEF} = V_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot \mathrm{BW}}} \qquad (2)$$

where $V_{ni,rms}$ is the input-referred rms noise voltage, I_{tot} is the total amplifier supply current, U_T is the thermal voltage kT/q, and BW is the amplifier bandwidth. See, for example, the disclosure of Steyaert et al. (discussed above). In formula (2), an amplifier using a single bipolar transistor (with no $1/f$ noise) has an NEF of one. All practical circuits, however, have values higher than 1.

[38] Substituting the expression for amplifier thermal noise integrated across the bandwidth BW from formula (1) into formula (2), and assuming that g_{m3} and g_{m7} are substantially less than g_{m1} (i.e., by a factor of about 10 to 20), the NEF can be represented by formula (3):

$$\mathrm{NEF} = \sqrt{\frac{2\gamma I_{tot}}{U_T g_{m1}}} = \sqrt{\frac{8\gamma}{U_T}\left(\frac{I_{D1}}{g_{m1}}\right)} \qquad (3)$$

where I_{D1} is the drain current through M_1 (which is ¼ of the total amplifier supply current). Thus, to minimize the NEF, the relative transconductance g_m/I_D of transistors M_1 and M_2 should be maximized.

[39] In conditions of weak inversion, the relative transconductiance g_m/I_D reaches its maximum value of κ/U_T. Under such conditions, the size of transistors M_1 and M_2 $[(W/L)_1]$ are made large enough to ensure sub-threshold operation of the OTA with

microamp current levels. Using the model for thermal noise valid in weak inversion described in Y. Tsividis (discussed above), NEF can be represented by formula (4):

$$\mathrm{NEF} = \sqrt{\frac{4}{\kappa U_T}\left(\frac{I_{D1}}{g_{m1}}\right)} \qquad (4)$$

where κ is the sub-threshold gate coupling coefficient. In conditions of weak inversion, the expression for NEF reduces to formula (5):

$$\mathrm{NEF} = \sqrt{\frac{4}{\kappa^2}} \cong 2.9 \qquad (5)$$

assuming a typical value of $\kappa = 0.7$. Formula (5) represents the theoretical NEF limit for an amplifier with the circuit topology illustrated in Figure 1 and Figure 3 that has been constructed from MOS transistors. The NEF derived in formula (5) will, of course, be limited by constraints on g_{m3} and g_{m7} as discussed above, as well as by $1/f$ noise.

[40] In other aspects of the invention, such as where the amplifier has a different circuit topology, the NEF will be different. As well, the optimum transistor size and other parameters of the amplifier will be different.

[41] EXAMPLE

[42] An amplifier in a 1.5μm 2-poly commercially-available CMOS process was fabricated to be a fully-integrated circuit of dimensions 250μm by 700μm on a chip with dimensions of 2.2mm by 2.2mm. No external components such as capacitors or resistors are necessary for the circuit operation; all necessary circuit components are contained on the chip as an integrated circuit having dimensions of less than 1mm by 1mm. The amplifier was designed for a gain of 100, setting C_1 to 20pF and C_2 to 200fF. Figure 4

shows the measured amplifier transfer function from 0.7Hz to 50kHz. The midband gain was measured to be 39.5dB, slightly lower than the designed specification of 40dB. This discrepancy is likely caused by fringing fields on the small C_2 capacitors, yielding a larger capacitance than designed. Figure 5 shows the output of the amplifier in response to a 0.006Hz square wave. Based on the slow adaptation of the output, the low-frequency cutoff f_L was estimated to be approximately 0.1mHz.

[43] Figure 6 shows the measured input-referred noise power spectral density (PSD). The thermal noise power was $21\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ and the $1/f$ noise corner occured at 100Hz. Integration under this curve yielded an rms noise voltage of 2.2μVrms. This noise measurement was confirmed by recording the output noise waveform and dividing by the gain to generate an input-referred noise waveform whose rms value was 2.2μVrms as depicted in Figure 7. Table I compares these (and other) measurements along with the simulated results.

TABLE I
SIMULATED AND MEASURED CHARACTERISTICS OF AMPLIFIER

Parameter	Simulated	Measured
Supply voltage	±2.5 V	±2.5 V
Supply current	16 μA	16 μA
Gain	40 dB	39.5 dB
Bandwidth	7.5 kHz	7.2 kHz
Low-frequency cutoff	130 mHz	~0.1 mHz
Input-referred noise	3.1 μVrms	2.2 μVrms
Noise efficiency factor	5.6	4.0
THD (16.7 mVpp input)	*	1.0%
Dynamic range (%1 THD)	*	69 dB
CMRR (10 Hz – 5 kHz)	≥ 42 dB	≥ 83 dB
PSRR (10 Hz – 5 kHz)	≥ 42 dB	≥ 85 dB
Crosstalk (f = 1 kHz)	*	-64 dB
Area (in 1.5μm technology)	n/a	0.17 mm^2

*Not Measured

[44] The simulated noise levels exceeded those measured due to conservative estimates of $1/f$ noise coefficients. The NEF of the amplifier was 4.0, substantially near the theoretical limit of 2.9 calculated in formula (5). The distortion remained below 1% THD for inputs less than 16.7mV peak-to-peak (larger than typical extracellular neural signals). The dynamic range was calculated assuming a distortion limit of 1% (a conservative definition) as 69dB. Crosstalk was measured between amplifiers adjacent on the chip, and was -64dB or less.

[45] Figure 8 shows the power-noise performance of this amplifier compared with estimated NEF values from conventional bioamplifiers. The amplifier of this Example presented here exhibits a better NEF than these conventional designs.

[46] Having described the preferred aspects of the invention, it is understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.